

ORCAD SIGNAL EXPLORER

OrCAD® Signal Explorer provides a scalable, cost-effective pre- and post-route signal integrity (SI) analysis and board-level topology exploration environment for complex printed circuit boards (PCBs). It enables signal exploration, analysis, and validation, allowing designers to increase circuit reliability and drive known good interconnect requirements throughout the design process.

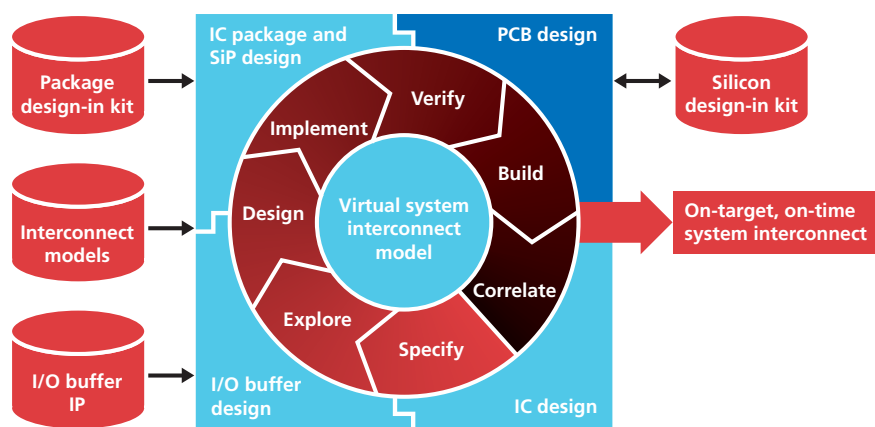


Figure 1: The affordable, high-performance OrCAD product line is easily scalable with the full complement of Cadence Allegro PCB design solutions

ORCAD PCB DESIGN TECHNOLOGIES

OrCAD products have a proven track record of innovation in the PCB personal productivity market. Available as stand-alone tools or in comprehensive suites, they allow designers to realize products from conception to manufacturing output. Easy-to-use and intuitive, they offer exceptional value. OrCAD technology also provides easy migration to the Cadence® Allegro® platform (see Figure 1).

INTEGRATED, COST-EFFECTIVE SI TECHNOLOGY

Increasing design density, complexity, and faster edge rates create a multitude of SI issues, which can impact design schedules and lead to increases in production costs. To avoid costly, time-consuming and frustrating simulate-fix-simulate iterations, designers have to address SI issues throughout the design process—from the very beginning of the cycle through placement and final routing.

OrCAD Signal Explorer helps engineers achieve exactly this goal. It enables them to explore topologies and models with manufacturing tolerances, weigh the trade-offs involved in routing choices, and use optimal constraints to drive the physical layout and routing of the PCB design. It then makes it easy to perform post-layout extraction and verification of complex PCB interconnect.

Tight integration with OrCAD PCB Editor eliminates database conversion and possible translation issues. Engineers can now perform SI analysis or topology exploration at any stage of the design cycle—when the board is partially or fully placed, partially or fully routed, and even when no netlist or PCB database exists.

BENEFITS

- Increases circuit reliability
- Improves circuit performance
- Reduces number of prototypes
- Enables pre- and post-route signal integrity analysis
- Eliminates need to translate design databases to run simulations
- Provides full scalability to Allegro PCB SI products

FEATURES

SIGXPLOER MODULE

OrCAD Signal Explorer uses a graphical topology design and editing canvas, SigXplorer, that allows design engineers to prototype critical signal connectivity, understand sensitivity, and use “what-if” scenarios to develop optimal interconnect strategies. SigXplorer allows users to analyze and validate topologies against SI requirements and constraints. It can be used for pre-route topology design and analysis even before a schematic is created. By performing this type of analysis at the earliest stages of the design cycle, designers can assess the impact of using a new device technology or of increasing edge rates.

With SigXplorer designers can build and validate detailed electrical topology models and prove the viability of a new technology—before the detailed design process begins. OrCAD Signal Explorer can directly extract an electrical view of a physical topology, including interconnect artifacts such as vias and changes in interconnect that affect impedance or velocity. This allows the design engineer to perform “what-if” investigations of electrical behavior without having to edit the PCB design. The

engineer can investigate the effects of changing parameter values and develop an acceptable solution without disrupting the PCB design process. This ability is available at any stage of the PCB design process, from placement through to a fully routed board. (See Figure 2.)

SIMULATION ENVIRONMENT

OrCAD Signal Explorer provides a SPICE-based simulation environment for PCB SI analysis. It consists of the Tlsim simulation engine, the SigWave waveform display, the Device Modeling Language (DML), translators from other modeling formats, and a library model editing/management subsystem.

The Tlsim simulation engine combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. It includes an IBIS-style behavioral driver element that models I/O behavior based on the V-I and V-T data provided by behavioral modeling techniques. By combining both structural and behavioral modeling techniques, Tlsim enables accurate and efficient modeling of complex device behavior. It includes a lossy, frequency-dependent transmission line model that accurately predicts the distributed behavior of PCB traces up to several GHz. An integrated electrical field solver is used to determine the electrical characteristics of routed etch and to create electrical models of PCB vias.

The SigWave module provides capabilities to import waveform data both directly from various standard test equipment formats as well as from the output formats of popular SI analysis tools. The SigWave waveform viewer can present simulation results in multiple formats.

- *Oscilloscope mode* allows users to turn the display of individual waveforms on and off, provides markers for use in making on-screen measurements, and allows notes to be added to the display

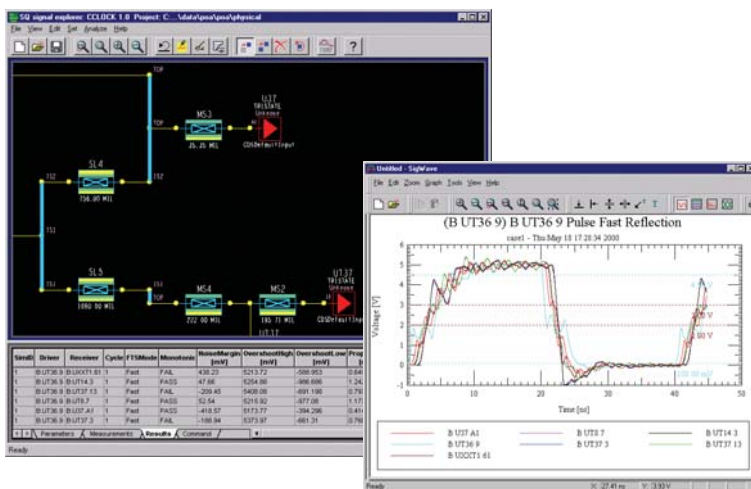


Figure 2: OrCAD Signal Explorer analyzes and validates topologies and interconnects to help minimize potential SI-related issues for fewer re-spins and shorter lab debug time

- *Logic-analyzer mode* presents waveforms alongside each other so that logic behavior and bus transactions are easier to observe
- *Spectrum analyzer mode* displays signal behavior in the frequency domain using one of several different FFT techniques
- *Eye-diagram mode* is useful for viewing patterns in long simulation sequences

MODEL INTEGRITY MODULE

The Model Integrity module allows engineers to create, manipulate, and validate models quickly in an easy-to-use editing environment. It provides a model browser and syntax checker for models written in IBIS as well as for advanced models written in DML. The marker navigation functionality provides an easy way to fix syntax errors. Engineers can use SigXplorer to verify models with simple test circuits.

OrCAD Signal Explorer accepts device models from a variety of digital modeling formats. Support for the IBIS 4.1 modeling standard allows OrCAD Signal Explorer to use models created by most semiconductor manufacturers. Users can also translate models from the Mentor/Quad XTK simulator format or create models from SPICE device models. In addition, OrCAD Signal Explorer includes a next-generation modeling language (DML) for more complex devices. This flexible macro modeling extension language augments IBIS and allows state-of-the-art I/O functionality to be modeled quickly and accurately.

WAVEFORM VIEWER

The Waveform View enables graphical browsing of waveforms. It features:

- Simple on/off control for waveforms display
- Line font and color controls
- Alternate spreadsheet data view
- Customization for scaling and labeling of axes
- Easy adjustment of voltage threshold for different technologies

SCALABILITY PATH

Unlike other SI solutions, OrCAD Signal Explorer is a feature-rich, fully scalable solution. As SI challenges and design sophistication grow, OrCAD Signal Explorer grows with them, providing an easy upgrade path from the OrCAD product line to the Allegro PCB SI L, XL, and GXL series—without the need to translate, learn new applications, or change use models.

SYSTEM REQUIREMENTS

- Pentium 4 (32-bit) equivalent or faster
- Windows XP Professional, Windows XP Home Edition, Windows 2000 (SP4), or Windows Server 2003
- Minimum 256MB RAM (512MB or more recommended)
- 300MB swap space (or more)
- CD-ROM Drive
- 32,768 color Windows display with minimum 1024 x 768 (1280 x 1024 recommended)

SALES, TECHNICAL SUPPORT, AND TRAINING

The OrCAD product line is owned by Cadence Design Systems, Inc. and supported by a worldwide network of Cadence Channel Partners. For sales, technical support, or training, contact your local Cadence Channel Partner. For a complete list of authorized Cadence Channel Partners, visit www.cadence.com/partners/channel_partner/index.aspx.

PRICING INFORMATION

For product pricing and availability, contact a Cadence Channel Partner nearest you. For a complete list of authorized Cadence Channel Partners, visit www.cadence.com/partners/channel_partner/index.aspx.