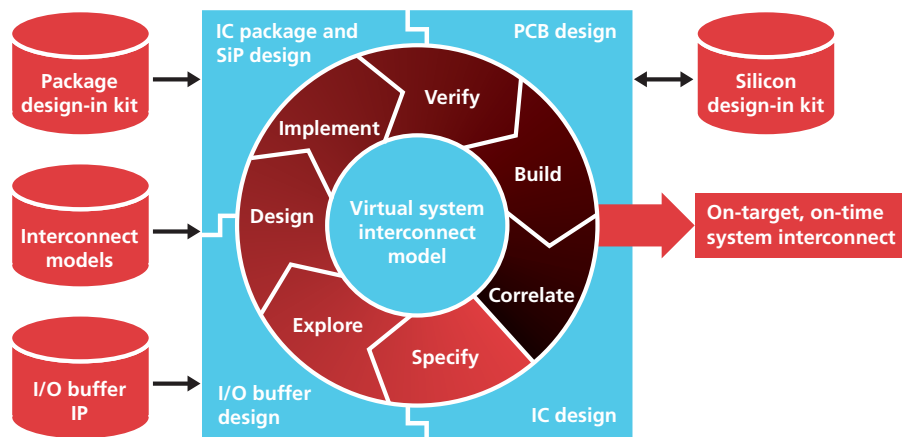


ALLEGRO SYSTEM ARCHITECT GXL

Cadence® Allegro® System Architect GXL is the industry’s first multi-style design creation environment. It provides the flexibility and power to create complex system designs using spreadsheets, traditional schematics, or HDL (Verilog®). Compared with conventional schematic capture systems, Allegro System Architect GXL significantly reduces the time to create designs. It is especially effective for complex designs and those with large pin-count devices.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

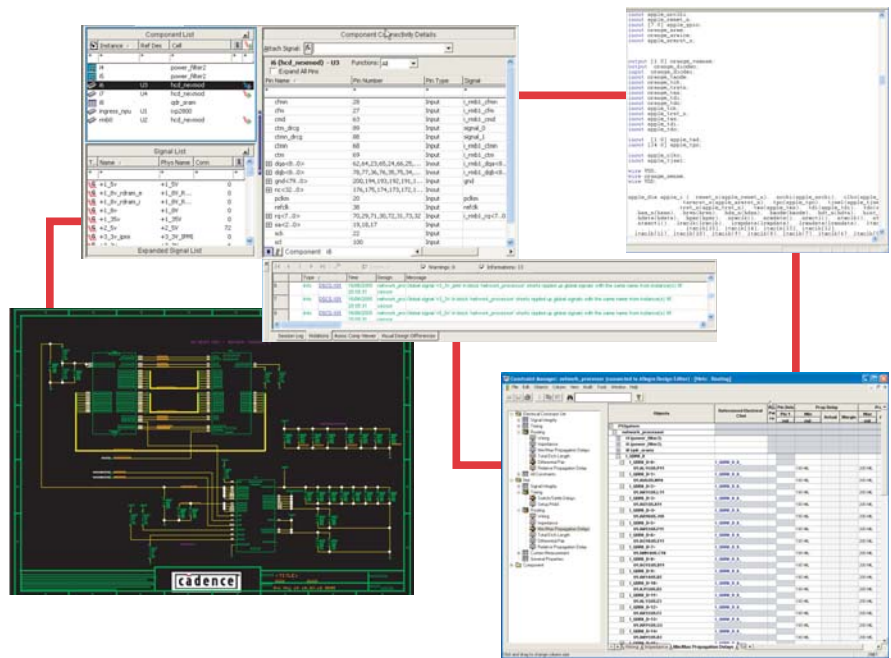
ALLEGRO SYSTEM ARCHITECT GXL

Allegro System Architect GXL lets designers create complex systems faster by allowing them to use a design style most appropriate for the design type. In addition to traditional schematic-based design capture, two new paradigms for creating system designs—spreadsheets and HDL—give users the power to tackle designs with large-pin-count devices. The ability to create different parts of the same design using different paradigms, individually or as part of a team, shortens creation time. Allegro System Architect GXL allows multiple designers to work concurrently on a project, regardless of team proximity. Additionally, full integration into the Allegro system interconnect design platform provides reliable physical realization of the system.

Allegro System Architect GXL does not require schematic symbols to create design intent to drive connectivity to the PCB Editor. This reduces symbol library dependencies for critical projects. The ability to include schematic blocks and use schematic libraries allows designers to reuse old designs and protect their current library investment.

BENEFITS

- Shortens time to create designs
- Eliminates the need for schematic symbols
- Reduces support costs through customized report generation and localization options
- Provides intuitive GUI to reduce learning curve
- Allows multiple designers and layout engineers to work in parallel
- Generates schematics automatically, eliminating the need to draw them



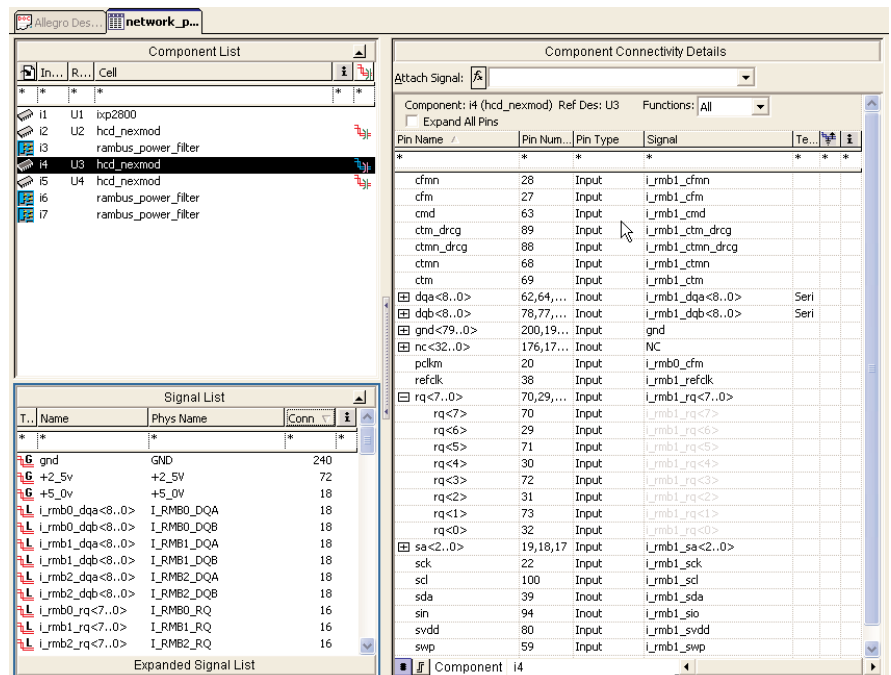
Multi-style design creation environment integrating spreadsheets, HDL (Verilog), and schematics

FEATURES

SPREADSHEET EDITOR

Customized for system design, the spreadsheet editor provides many productivity enhancements including powerful sort, filter, search, and copy/paste capabilities. It is available in two viewing modes—component-based view and net-based view. This allows users to edit the connectivity of

multiple components at the same time as well as simplifying signal travel and debugging. It is highly customizable—providing the flexibility to display content and order elements as required. This not only makes editing connectivity for large-pin-count devices much simpler, designers no longer have to add multiple symbols across many sheets.



Intuitive spreadsheet editor showing component list, signal list, and connectivity details

A special matrix view allows users to observe the connectivity of multiple components and signals in a single table. This is ideal, for example, when looking at a specific bus interface.

ASSOCIATED COMPONENTS

The large number of discrete components—series and shunt terminators, pull-up/pull-down resistors, and decoupling capacitors—that accompany large-pin-count devices can take a huge amount of time to wire up in a schematic. To make managing these discrete devices easier, Allegro System Architect GXL provides special features to connect and associate them with the large-pin-count devices, and to pass the associations to Allegro PCB Editor.

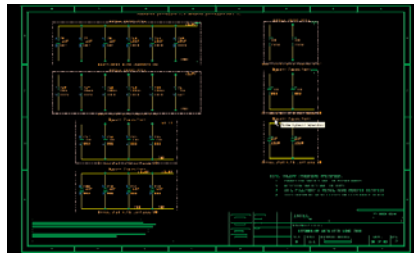
INTEGRATED CONSTRAINT MANAGEMENT

Allegro Constraint Manager handles design constraints and properties with features that include real-time topology apply, integration with Allegro Signal Explorer, and access to all design objects including extended nets, differential pairs, buses, and matched groups. Advanced features include the ability to automatically extract and use constraints from blocks added to the design.

REPORTS AND SCHEMATIC GENERATION ENGINE

A report engine provides easy extraction of design information and presents the data in a variety of formats. It allows designers to use existing design relationships in queries and export reports in various formats including HTML, CSV, and tab-separated text. These editable design report files also include the ability to cross-probe to nets and components in the design.

The schematic generator has been enhanced to generate compact schematics and allow users to make placement changes in generated schematics, which are preserved for future runs.



Schematic generator is customized for PCB design with many features such as generating rails for bypass capacitors

PCB EDITOR INTEGRATION

Allegro System Architect GXL is fully integrated with Allegro PCB Editor, an interactive, high-speed, constraint-driven environment for creating and editing complex, multilayer PCBs. Its extensive feature set addresses a wide range of design and manufacturability concerns. An advanced design differencing capability synchronizes changes made in logic design and layout. An intelligent collection manager processes differences to make sure that change information is presented in a hierarchical and easy-to-use UI without duplication. A full two-way connectivity upgrade flow is supported, making it ideal for routing studies, FPGA, and package designs.

OTHER FEATURES

- Ability to use existing design libraries
- Ability to import and integrate schematic blocks in spreadsheet designs
- Verilog language sensitive editor
- Import schematic blocks
- Online DRC
- Online packaging
- Component Search, Global Navigate
- Global Find and Replace
- High-speed integration support for extended nets, differential pairs, buses
- Associated component support (terminations, bypass, pull-ups)
- Schematic generation with preserve options
- Advanced design differences engine with controlled update
- Team design and design reuse (including physical reuse)

OPERATING SYSTEM SUPPORT

- Red Hat Linux 7.3, 8.0, RHEL 3.0
- Windows 2000 with Service Pack 4, XP Professional
- Sun Solaris 8, 9
- HP-UX 11.0, 11.11i
- IBM AIX 5.1

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or Cadence Channel Partner in your area, visit www.cadence.com/contact_us.