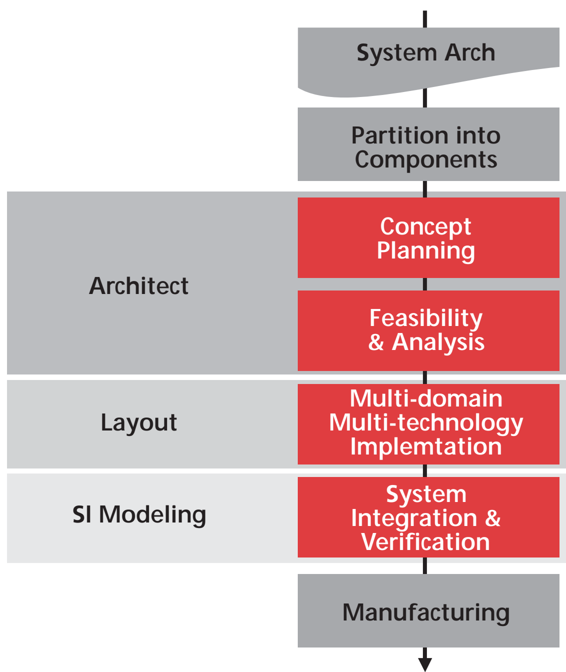
DATASHEET

cadence

CADENCE SIP DIGITAL LAYOUT

While system-in-package (SiP) design allows electronics makers to pack more functionality into a smaller footprint, it often involves highly complex combinations, such as stacked wirebond die, wirebond die stacked on flip-chip die, direct die-to-die attachment, and others. Cadence® SiP Digital Layout addresses this complexity by providing a complete constraint- and rules-driven package substrate layout environment that supports all packaging methods, including PGA, BGA, micro-BGA, chip scale, as well as flip-chip and wirebond attach methods.



The Cadence SiP design technology provides a methodology, flow and toolset for the definition, implementation and verification of multi-chip and multi-component IC packages

CADENCE SIP DESIGN TECHNOLOGY

Manufacturers of high-performance consumer electronics are turning to SiP design because it can provide a number of advantages over SoC. In addition to reduced cost, lower power, and higher performance, SiP design offers the flexibility to mix RF and high-speed digital circuitry in the same package. However, this also means it requires expert engineering talent in widely divergent fields. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), the Cadence SiP design technology streamlines the integration of multiple high-pin-count chips onto a single substrate. This approach allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development. Cadence SiP solutions

seamlessly integrate into Cadence Encounter® for die abstract co-design, Cadence Virtuoso® for RF module design, and Cadence Allegro® for package/board co-design.

SIP DIGITAL LAYOUT

As key component of the Cadence SiP design technology, Cadence SiP Digital Layout provides a constraint- and rules-driven layout environment for SiP design. This includes substrate place and route, final connectivity optimization at the IC, substrate, and system levels, manufacturing preparation, full design validation, and tapeout. The environment features integrated IC/package I/O planning capabilities and three-dimensional (3D) die stack creation and editing capabilities.

In addition, full online design-rule checking (DRC) supports the complex and unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. Multi-layer flip-chip along with radial any-angle routing substrate routing provide rapid constraint-driven interconnect creation.

BENEFITS

- Provides 3D die stack creation/editing for rapid stack assembly and optimization
- Enables IC I/O pad ring/array co-design and connectivity optimization at the IC, substrate, and system levels
- Allows connectivity assignment and optimization between ICs and substrate for optimized/minimal layer usage based on signal integrity and routability
- Reduces tedious, time-consuming, and manual breakout editing via flip-chip die autoroute-breakout
- Includes comprehensive substrate DFM capabilities for rapid design manufacturing preparation
- Provides 3D design viewer and DRC for accurate full 3D wire bondability verification, design review debug, and design documentation for assembly and test

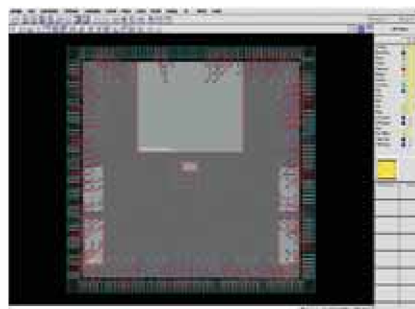
FEATURES

ALLEGRO CONSTRAINT MANAGER

Integrated constraint management provides the definition, application, and management of interconnect constraints and topologies at the physical prototyping and implementation level. Designers can import constraints and apply them to industry standard buss protocols—such as PCI-Express and DDR2—through hierarchical interconnect topology templates that are available from Cadence as well as various IC vendors.

I/O PLANNER

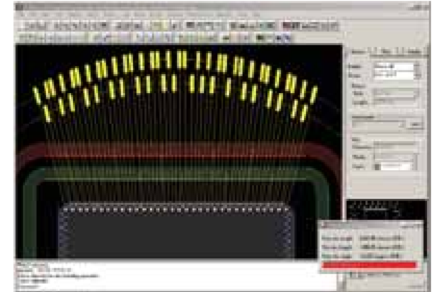
The IC die abstract I/O Planner provides the definition and optimization of co-design die bump matrix, I/O pad ring/array through connectivity assignment, I/O placement, and redistribution layer (RDL) routing. It can create either a die abstract from scratch, or load an abstract from the digital IC design team (LEF/DEF or OA), and then optimize it in the context of the SiP substrate as well as other IC die in the design. The I/O Planner is based on Cadence Encounter technology, which not only assures 100 percent compatibility with the chip design teams IC flow but also provides complete IC technology file compliance.



I/O Planner provides concurrent co-design of IC die padring/arrays and package substrate

SUBSTRATE EDITOR

The substrate Place and Route Editor allows the package layout designer to physically implement a SiP design based on the final chosen concept. It provides a full rules-driven, connectivity-based capability that ensures a correct-by-construction approach. The die abstracts, discrete components, and connectivity and constraint data are used to build the physical SiP implementation. The package layout designer can then use intuitive graphical editing tools to implement the design and prepare it for manufacture. It also supports all packaging methods: PGA, LGA, BGA, micro-BGA, and chip scale, as well as flip-chip and wirebond attach methods.

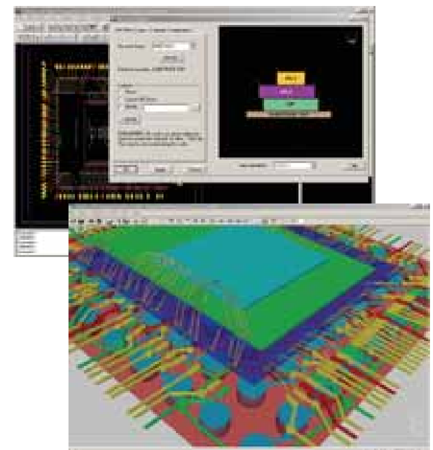


Interactive, dynamic wirebond design capability

An embedded, push-button, full 3D quasi-static field solver provides the extraction and creation of detailed, accurate geometric RLC or S-Parameter package simulation models for use during PCB design.

3D DIE STACK EDITOR

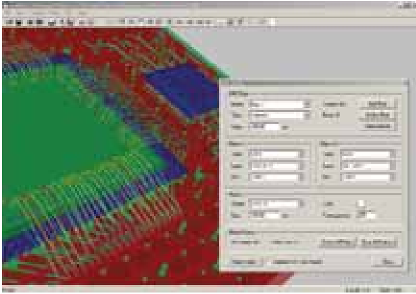
The Die Stack Editor provides a 3D construction environment for assembling complex die stacks. Die stacks are instantiated on the two-dimensional (2D) substrate design as hierarchical design objects.



The Die Stack Editor enables accurate 3D stacking and design placement

3D DESIGN VIEWER

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as a die stack or complex via array. Additionally, it provides a common reference point for design reviews.



3D design viewer and wirebond DRC capability ease design reviews and simplify complex bondshell pattern checking

OTHER SIP DIGITAL SOLUTION PRODUCTS

SIP DIGITAL ARCHITECT

This solution provides the project architect and design team with an environment for the exploration, definition, capture, construction and validation of design concept feasibility prior to final physical detailed implementation. Built around a unique System Connectivity Manager, it provides the architect with a unique environment to explore and define system connectivity/functionality that is optimized between ICs, SiP substrate, and target PCB system. It fully supports IC-driven or package/PCB substrate-driven flows with cross fabric domain ECO and LVS validation.

SIP DIGITAL SI

This tightly integrated interconnect signal integrity analysis and modeling solution is built around an SI-focused substrate editor for advanced IC packages. It is architected to handle a range of designs—from those with a large number of high-speed signals to designs that have signals operating in the multi-gigahertz (MGH) range. For today's serial interface designs (SERDES) it offers complete, integrated S-Parameter support and fast (10,000 bits in seconds) high-capacity simulation for jitter and bit-error-rate prediction.

SPECIFICATIONS

SYSTEM REQUIREMENTS

- OpenGL graphics compliance with a minimum of 64MB of dedicated memory

PLATFORM/OS

- Solaris
- Linux
- HP-UX
- MS Windows XP

INTERFACES

- LEF/DEF 5.1 to 5.6 (die abstract creation/export)
- OA 2.2 (die abstract creation/import)
- DXF
- GDSII
- AIF2
- Gerber 274X

3RD-PARTY SUPPORT

- Connections Program integration with:
- Optimal O-Wave for 3D full wave extraction and modeling
- Ansys PTD for full SiP substrate thermal analysis and modeling

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

SIP FEATURE SUMMARY

	SiP Digital Architect GXL	SiP Digital ArchitectXL	SiP Digital Layout GXL	SiP Digital SI XL	SiP RF Architect XL	SiP RF Layout GXL
Front-end Design Creation Features						
Virtuoso Analog Design Environment, schematic and layout integration & flow					x	
Substrate level embedded RF passive synthesis					x	
System Connectivity Manager	x	x				
Full SiP LVS (substrate and IC's)	x	x				
Signal Integrity Features						
SigXplorer topology editor and simulator (pre-route capabilities)	x			x		
SigXplorer topology editor and simulator (pre and post route capabilities)				x		
S-parameter interconnect modeling and SI simulation	x			x		
3D PCB package simulation model creation	x		x	x		x
Quasi-static 3D extraction/modeling engine	x			x		
Spectre simulation engine	x			x		
Channel analysis for high-capacity SI simulation	x			x		
Package/pin delay length report	x		x	x		x
Substrate Design Features						
Constraint Manager (Electrical and Physical)	x	x	x	x		x
Export SiP design to .mcm	x		x			x
Interactive (i/a) and automatic component (packaged and bare die) placement	x		x	i/a only		x
Auto/interactive Wirebonding	x		x	x		x
Full and partial design connectivity assignment and optimization (Router based, closest match and interactive and constraint based)	x		x	x		x
Interactive and automatic interconnect routing (free angle and multilayer orthogonal)	x		x	x		x
On-line soldermask checking			x			x
Recursive breakout pattern creator	x		x			x
Static style screen rulers						x
Advanced Design Features						
I/O Planning co-design editor (using LEF/DEF & OA2.2)	x		x			x
Hierarchical GDS2 output			x			x
Embedded RF passive creation and editing						x
3D Design Viewer & 3D wirebond DRC	x		x	x		x
3D Die Stack Editor	x		x			x
Interconnect Cline spreading			x			x
Tiles creation, editing	x		x			x
BGA Editor	x		x	x		x
HDI Via structure support	x		x	x		x
DFM Preparation/Output						
Die/BGA footprint compare using DEF/OA/.TXT	x		x			x
Filled shapes (metal) creation and editing			x	x		x
Design documentation such as dimensioning, annotation			x			x
Etch back of plating traces			x			x
Plating bar generation			x			x
Manufacturing / documentation export/import capabilities (stream, dxf, AIF etc)			x			x
Substrate mask output (Gerber, GDS2)			x			x
Full design status reporting capabilities	x		x	x		x
Waived DRC's (creation and reporting)	x		x	x		x
Degassing of filled metal shapes			x			x
Thieving (metal area balancing)			x			x

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223
or visit www.cadence.com for
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