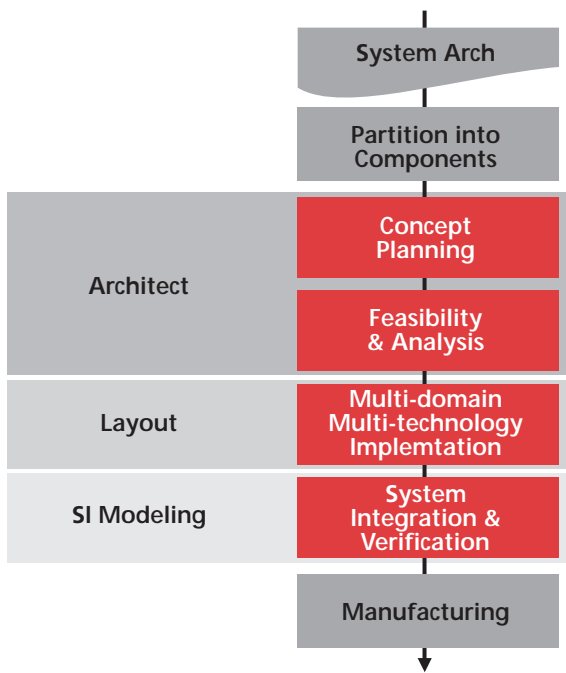


CADENCE SiP RF LAYOUT

While system-in-package (SiP) design makes it possible to combine RF and analog content on the same substrate, it presents a number of challenges. These include designing and integrating RF/analog chips with substrate-level buried RF passive devices as well as enabling top-level pre- and post-layout circuit simulation of the entire SiP design. Cadence® SiP RF Layout provides the proven path between Virtuoso® analog design/simulation and substrate layout. It enables layout designers to implement a SiP RF design that includes RF/analog die, embedded RF discrettes, constraint-driven interconnect routing, and full SiP tapeout manufacturing preparation.



The Cadence SiP design technology provides a methodology, flow and toolset for the definition, implementation, and verification of multi-chip, and multi-component IC packages

CADENCE SiP DESIGN TECHNOLOGY

Manufacturers of high-performance consumer electronics are turning to SiP design because it can provide a number of advantages over SoC. In addition to reduced cost, lower power, and higher performance, SiP design offers the flexibility to mix RF and high-speed digital circuitry in the same package. However, this also means it requires expert engineering talent in widely divergent fields. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), the Cadence SiP design technology streamlines the integration of multiple high-pin-count chips onto a single substrate. This approach allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development. Cadence SiP solutions

seamlessly integrate into Cadence Encounter® for die abstract co-design, Cadence Virtuoso for RF module design, and Cadence Allegro® for package/board co-design.

SIP RF LAYOUT

SiP RF Layout provides a complete Virtuoso schematic-, constraint-, and rules-driven package substrate layout environment for SiP design. It features integrated I/O planning co-design capabilities and three-dimensional (3D) die stack creation and editing. All packaging methods, including PGA, BGA, micro-BGA, and chip scale as well as flip-chip and wirebond attach methods are supported. SiP RF Layout is based on a co-design process that enables the management of physical, electrical, and manufacturing interfaces between design components across all associated design fabrics, allowing designers to make tradeoffs and optimize the entire system interconnect. Full online design-rule checking (DRC) supports the complex and unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. Multiple cavities, complex shapes, and interactive and automatic wirebonding are all supported.



Intelligent RF embedded passive structures can be physically created or synthesized from target values

BENEFITS

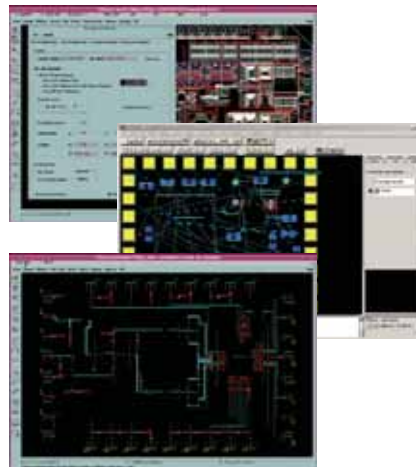
- Provides bi-directional engineering change order (ECO) and layout versus schematic (LVS) flow between RF design teams and SiP RF module layout team

- Supports substrate-level RF passive P-cell through Virtuoso top-level-driven design
- Allows direct import of SiP substrate-ready IC die footprints from Virtuoso Layout Editor
- Speeds die stack assembly and optimization with 3D creation/editing
- Provides IC I/O padding/array co-design and connectivity optimization at the IC, substrate, and system level
- Allows signal integrity (SI) and routability-driven connectivity assignment and optimization between ICs and substrate for optimized/minimal layer usage
- Reduces tedious, time consuming manual breakout editing via flip-chip die autoroute-breakout
- Includes comprehensive substrate DFM capabilities for rapid design manufacturing preparation
- Features 3D design viewer and DRC for accurate full 3D wire bondability verification, design review debug, and design documentation for assembly and test

FEATURES

INTEGRATED DESIGN FLOW

The single, integrated design flow is built around, and directly integrated into, the Virtuoso DFII framework. It features a single system-level, simulation-ready Virtuoso schematic for RF/analog die, SiP substrate, and packaged and embedded discret



Integrated design flow from Virtuoso circuit-simulation to substrate layout

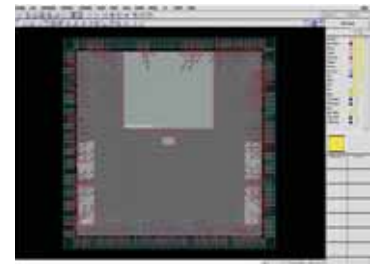
including substrate-level RF P-cell creation. It allows for direct export of SiP-level IC die footprints from Virtuoso Layout Editor.

CONSTRAINT MANAGER

Integrated constraint management provides the definition, application, and management of interconnect constraints and topologies at the physical prototyping and implementation level. Constraints can be imported and applied to industry- standard buss protocols, such as PCI-Express and DDR2, through hierarchical interconnect topology templates that are available from Cadence as well as various IC vendors.

I/O PLANNER

The IC die abstract I/O Planner provides the definition and optimization of co-design die bump matrixes, I/O padding/array through connectivity assignment, I/O placement, and redistribution layer (RDL) routing. It can create either a die abstract from scratch, or load an abstract from the digital IC design team (LEF/DEF or OA), and then optimize it in the context of the SiP substrate as well as other IC die in the design. The I/O Planner is based on Encounter technology, ensuring it is 100 percent compatible with the chip design team's IC tools and providing complete IC technology file compliance.



I/O Planner provides concurrent co-design of IC die padding/arrays and package substrate

SUBSTRATE EDITOR

The substrate Place and Route Editor allows the package layout designer to physically implement the SiP design based on the final chosen concept. It provides a full rules-driven, connectivity-based capability that

ensures a correct-by-construction approach. The die abstracts, discrete components, and connectivity and constraint data are used to build the physical SiP implementation. The package layout designer can then use the graphical, intuitive editing tools to implement the design and prepare it for manufacture. It supports all packaging methods, including PGA, LGA, BGA, micro-BGA, and chip scale as well as flip-chip and wirebond attach methods.

An embedded, push-button full 3D quasi-static field solver provides the extraction and creation of detailed, accurate geometric RLC or S-Parameter package simulation models for use during PCB design.



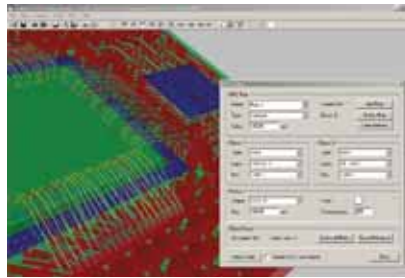
Comprehensive 2D assembly rule checks provide detailed SiP verification

3D DIE STACK EDITOR

The Die Stack Editor provides a 3D construction environment for assembling complex die stacks. Die stacks are instantiated on the two-dimensional (2D) substrate design as hierarchical design objects.

3D DESIGN VIEWER

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as a die stack or complex via array. It provides a common reference point for design reviews.



3D design viewer and wirebond DRC capability eases design reviews and simplifies complex bondshell pattern checking

OTHER SiP SOLUTION PRODUCTS

SiP RF ARCHITECT

SiP RF Architect provides a single integrated design flow built around the Virtuoso DFII framework. It enables a single, system-level, simulation-ready Virtuoso schematic for RF/analog die, SiP substrate, and packaged and embedded discretives. It allows direct export of SiP-level IC die footprints from Virtuoso Layout Editor and schematic-driven substrate-level RF parameterized cell (P-Cell) creation.

SiP DIGITAL SI

This tightly integrated interconnect SI analysis and modeling solution is built around an SI-focused substrate editor for advanced IC packages. It gives designers the ability to handle a range of designs—designs that have a large number of high-speed signals or designs having signals that operate in the multi-gigahertz (MGH) range. For today's serial interface designs (SERDES) it offers complete, integrated S-Parameter support, and fast (10,000 bits in seconds) high-capacity simulation for jitter and bit-error-rate prediction.

CADENCE RF SiP DESIGN METHODOLOGY KIT

The Cadence RF SiP Design Methodology Kit leverages new RF SiP technologies from Cadence and verified advanced methodologies. The kit enables wireless design teams to have predictable design schedules by increasing design productivity and quality, influencing first pass success. The kit delivers this verified methodology packaged in the RF SiP flow demonstrated on a segment representative design.

SPECIFICATIONS

SYSTEM REQUIREMENTS

PLATFORM/OS

- Windows XP
- Solaris
- Linux
- HP-UX

INTERFACES

- LEF/DEF 5.1 to 5.6

VIRTUOSO COMPATIBILITY

- CIC-4.x to 5.x

3RD-PARTY SUPPORT

- Agilent RFDE (ADS and MoMentum) for pre- and post-layout extraction and simulation

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (ILS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

SIP FEATURE SUMMARY

	SIP Digital Architect GXL	SIP Digital Architect XL	SIP Digital Layout GXL	SIP Digital SI XL	SIP RF Architect XL	SIP RF Layout GXL
Front-end Design Creation Features						
Virtuoso Analog Design Environment, schematic and layout integration & flow					X	
Substrate level embedded RF passive synthesis					X	
System Connectivity Manager	X	X				
Full SIP LVS (substrate and IC's)	X	X				
Signal Integrity Features						
SigXplorer topology editor and simulator (pre-route capabilities)	X			X		
SigXplorer topology editor and simulator (pre and post route capabilities)				X		
S-parameter interconnect modeling and SI simulation	X			X		
3D PCB package simulation model creation	X		X	X		X
Quasi-static 3D extraction/modeling engine	X			X		
Spectre simulation engine	X			X		
Channel analysis for high-capacity SI simulation	X			X		
Package/pin delay length report	X		X	X		X
Substrate Design Features						
Constraint Manager (Electrical and Physical)	X	X	X	X		X
Export SiP design to .mcm	X		X			X
Interactive (i/a) and automatic component (packaged and bare die) placement	X		X	i/a only		X
Auto/interactive Wirebonding	X		X	X		X
Full and partial design connectivity assignment and optimization (Router based, closest match and interactive and constraint based)	X		X	X		X
Interactive and automatic interconnect routing (free angle and multilayer orthogonal)	X		X	X		X
On-line soldermask checking			X			X
Recursive breakout pattern creator	X		X			X
Static style screen rulers						X
Advanced Design Features						
I/O Planning co-design editor (using LEF/DEF & OA2.2)	X		X			X
Hierarchical GDS2 output			X			X
Embedded RF passive creation and editing						X
3D Design Viewer & 3D wirebond DRC	X		X	X		X
3D Die Stack Editor	X		X			X
Interconnect Cline spreading			X			X
Tiles creation, editing	X		X			X
BGA Editor	X		X	X		X
HDI Via structure support	X		X	X		X
DFM Preparation/Output						
Die/BGA footprint compare using DEF/OA.TXT	X		X			X
Filled shapes (metal) creation and editing			X	X		X
Design documentation such as dimensioning, annotation			X			X
Etch back of plating traces			X			X
Plating bar generation			X			X
Manufacturing / documentation export/import capabilities (stream, dxf, AIF etc)			X			X
Substrate mask output (Gerber, GDS2)			X			X
Full design status reporting capabilities	X		X	X		X
Waived DRC's (creation and reporting)	X		X	X		X
Degassing of filled metal shapes			X			X
Thieving (metal area balancing)			X			X

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223
or visit www.cadence.com for
additional information.